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DS2143/DS2143Q
E1 Controller

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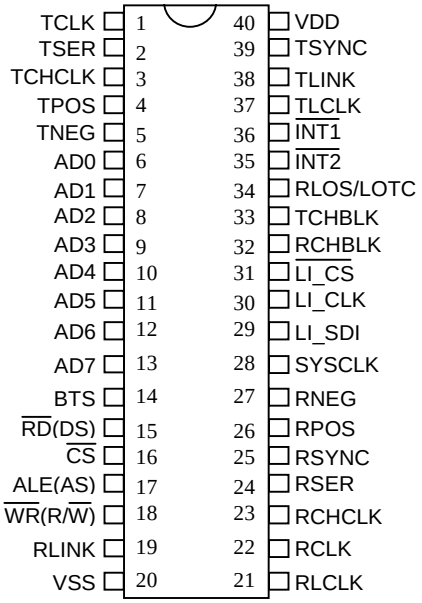
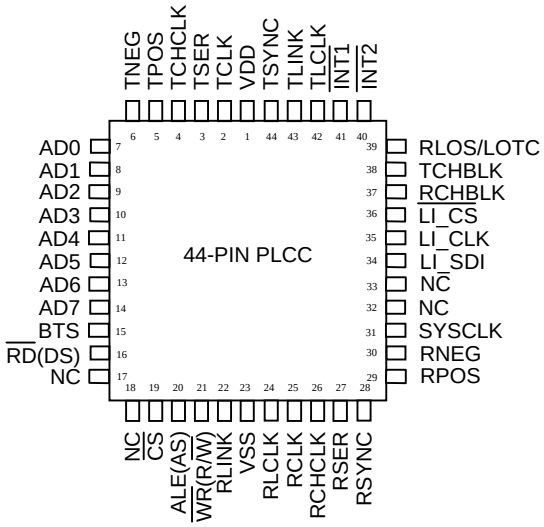
FEATURES

- E1/ISDN-PRI framing transceiver
- Frames to CAS, CCS, and CRC4 formats
- Parallel control port
- Onboard two frame elastic store slip buffer
- Extracts and inserts CAS signaling bits
- Programmable output clocks for fractional E1 links, DS0 loopbacks, and drop and insert applications
- Onboard Sa data link support circuitry
- FEBE E-Bit detection, counting and generation
- Pin-compatible with DS2141A T1 Controller
- 5V supply; low power (50 mW) CMOS
- Available in 40-pin DIP and 44-pin PLCC (DS2143Q)

PIN ASSIGNMENT



40-Pin DIP (600-mil)



DESCRIPTION

The DS2143 is a comprehensive, software-driven E1 framer. It is meant to act as a slave or coprocessor to a microcontroller or microprocessor. Quick access via the parallel control port allows a single micro to handle many E1 lines. The DS2143 is very flexible and can be configured into numerous orientations via software. The software orientation of the device allows the user to modify their design to conform to future E1 specification changes. The controller contains a set of 69 8-bit internal registers which the user

can access. These internal registers are used to configure the device and obtain information from the E1 link. The device fully meets al l of the latest E1 specifications, including CCITT G.704, G.706, and G.732.

1.0 INTRODUCTION

The DS2143 E1 Controller has four main sections: the receive side, the transmit side, the line interface controller, and the parallel control port. See the Block Diagram. On the receive side, the device will clock in the serial E1 stream via the RPOS and RNEG pins. The synchronizer will locate the frame and multiframe patterns and establish their respective positions. This information will be used by the rest of the receive side circuitry.

The DS2143 is an "off-line" framer, which means that all of the E1 serial stream that goes into the device will come out of it unchanged. Once the E1 data has been framed to, the signaling data can be extracted. The two-frame elastic store can either be enabled or bypassed.

The transmit side clocks in the unframed E1 stream at TSER and add in the framing pattern and the signaling. The line interface control port will update line interface devices that contain a serial port. The parallel control port contains a multiplexed address and data structure which can be connected to either a microcontroller or microprocessor.

Reader's Note:

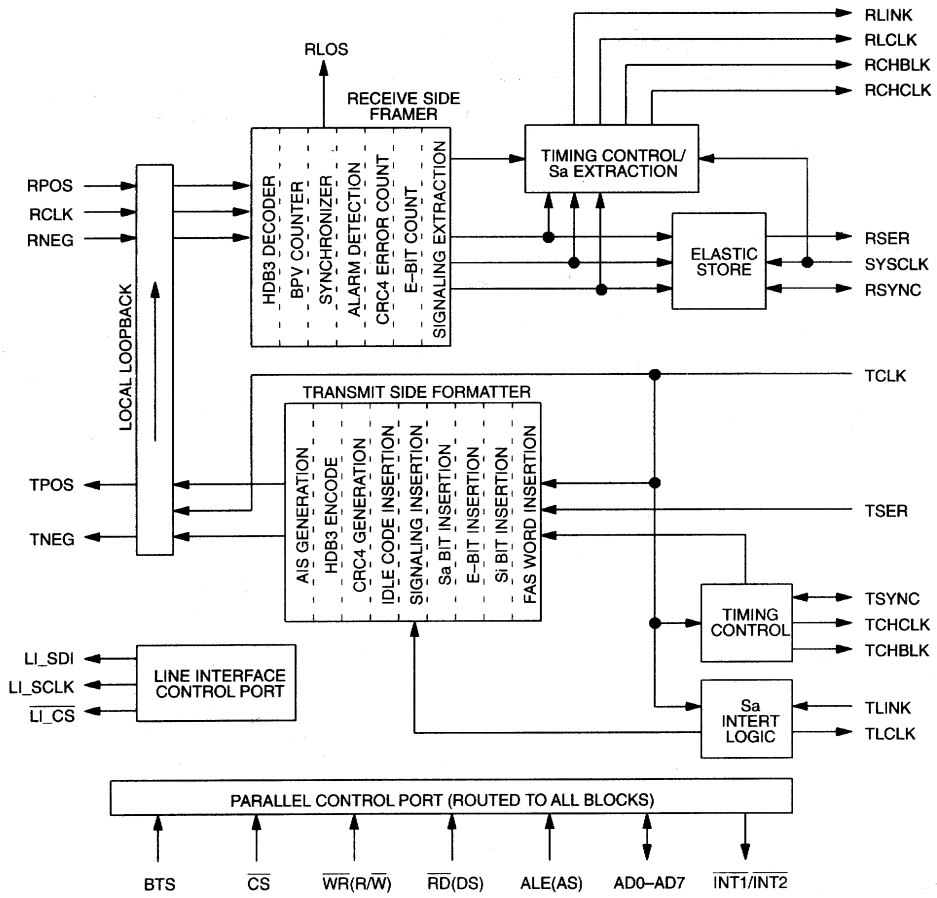
This data sheet assumes a particular nomenclature of the E1 operating environment. There are 32 8-bit timeslots in an E1 systems which are number 0 to 31. Timeslot 0 is transmitted first and received first. These 32 timeslots are also referred to as channels with a numbering scheme of 1 to 32. Timeslot 0 is identical to channel 1, timeslot 1 is identical to channel 2, and so on. Each timeslot (or channel) is made up of 8 bits which are numbered 1 to 8. Bit number 1 is the MSB and is transmitted first. Bit number 8 is the LSB and is transmitted last. Throughout this data sheet, the following abbreviations will be used:

FAS	Frame Alignment Signal
CRC4	Cyclical Redundancy Check
CAS	Channel Associated Signaling
CCS	Common Channel Signaling
MF	Multiframe
Sa	Additional bits
Si	International bits
E-bit	CRC4 Error Bits

DS2143 FEATURES

- Parallel control port
- Onboard two-frame elastic store
- CAS signaling bit extraction and insertion
- Fully independent transmit and receive sections
- Full alarm detection
- Full access to Si and Sa bits
- Loss of transmit clock detection
- HDB3 coder/decoder
- Full transmit transparency
- Large error counters
- Individual bit-by-bit Sa data link support circuitry
- Programmable output clocks
- Frame sync generation
- Local loopback capability
- Automatic CRC4 E-bit support
- Loss of receive clock detection
- G.802 E1 to T1 mapping support

DS2143 BLOCK DIAGRAM



PIN DESCRIPTION Table 1

PIN	SYMBOL	TYPE	DESCRIPTION
1	TCLK	I	**Transmit Clock.** 2.048 MHz primary clock. A clock must be applied at the TCLK pin for the parallel port to operate properly.
2	TSER	I	**Transmit Serial Data.** Transmit NRZ serial data, sampled on the falling edge of TCLK.
3	TCHCLK	O	**Transmit Channel Clock.** 256 kHz clock which pulses high during the LSB of each channel. Useful for parallel-to-serial conversion of channel data. See Section 13 for timing details.
4 5	TPOS TNEG	O	**Transmit Bipolar Data.** Updated on rising edge of TCLK. For optical links, can be programmed to output NRZ data.
6-13	AD0-AD7	I/O	**Address/Data Bus.** An 8-bit multiplexed address/data bus.
14	BTS	I	**Bus Type Select.** Strap high to select Motorola bus timing; strap low to select Intel bus timing. This pin controls the function of $\overline{RD}$ (DS), ALE(AS), and $\overline{WR}$ (R/$\overline{W}$) pins. If BTS=1, then these pins assume the function listed in parentheses ().
15	$\overline{RD}$ (DS)	I	**Read Input (Data Strobe).**
16	$\overline{CS}$	I	**Chip Select.** Must be low to read or write the port.
17	ALE(AS)	I	**Address Latch Enable (Address Strobe).** A positive-going edge serves to demultiplex the bus.
18	$\overline{WR}$ (R/$\overline{W}$)	I	**Write Input (Read/Write).**
19	RLINK	O	**Receive Link Data.** Outputs Sa bits. See Section 13 for timing details.
20	V_{SS}	-	**Signal Ground.** 0.0 volts.
21	RLCLK	O	**Receive Link Clock.** 4 kHz to 20 kHz demand clock for the RLINK output. Controlled by RCR2. See Section 13 for timing details.
22	RCLK	I	**Receive Clock**. 2.048 MHz primary clock. A clock must be applied at the RCLK pin for the parallel port to operate properly.
23	RCHCLK	O	**Receive Channel Clock**. 256 kHz clock which pulses high during the LSB of each channel. Useful for serial to parallel conversion of channel data. See Section 13 for timing details.
24	RSER	O	**Receive Serial Data**. Received NRZ serial data, updated on rising edges of RCLK.
25	RSYNC	I/O	**Receive Sync**. An extracted pulse, one RCLK wide, is output at this pin which identifies either frame (RCR1.6=0) or multiframe boundaries (RCR1.6=1). If the elastic store is enabled via the RCR2.1, then this pin can be enabled to be an input via RCR1.5 at which a frame boundary pulse is applied. See Section 13 for timing details.
26 27	RPOS RNEG	I	**Receive Bipolar Data Inputs**. Sampled on falling edge of RCLK. Tie together to receive NRZ data and disable BPV monitoring circuitry.
28	SYSCLK	I	**System Clock**. 1.544 MHz or 2.048 MHz clock. Only used when the elastic store function is enabled via the RCR2.1. Should be tied low in applications that do not use the elastic store.

PIN	SYMBOL	TYPE	DESCRIPTION
29	LI_SDI	O	**Serial Port Data for the Line Interface**. Connects directly to the SDI input pin on the line interface. See Sections 12 and 13 for timing details.
30	LI_CLK	O	**Serial Port Clock for the Line Interface**. Connects directly to the SCLK input pin on the line interface. See Sections 12 and 13 for timing details.
31	LI_ $\overline{\text{CS}}$	O	**Serial Port Chip Select for the Line Interface.** Connects directly to the $\overline{\text{CS}}$ input pin on the line interface. See Sections 12 and 13 for timing details.
32 33	RCHBLK TCHBLK	O	**Receive/Transmit Channel Block**. A user programmable output that can be forced high or low during any of the 32 E1 channels. Useful for blocking clocks to a serial UART or LAPD controller in applications where not all E1 channels are used such as Fractional E1 or ISDN-PRI. Also useful for locating individual channels in drop-and-insert applications. See Sections 9 and 13 for details.
34	RLOS/LOTC	O	**Receive Loss of Sync/Loss of Transmit Clock**. A dual function output. If TCR2.0=0, then this pin will toggle high when the synchronizer is searching for the E1 frame and multiframe. If TCR2.0=1, then this pin will toggle high if the TCLK pin has not toggled for 5 µs.
35	$\overline{\text{INT2}}$	O	**Receive Alarm Interrupt 2**. Flags host controller during conditions defined in Status Register 2. Active low, open drain output.
36	$\overline{\text{INT1}}$	O	**Receive Alarm Interrupt 1**. Flags host controller during alarm conditions defined in Status Register 1. Active low, open drain output.
37	TLCLK	O	**Transmit Link Clock**. 4 kHz to 20 kHz demand clock for the TLINK input. Controlled by TCR2. See Section 13 for timing details.
38	TLINK	I	**Transmit Link Data**. If enabled, this pin will be sampled on the falling edge of TCLK to insert Sa bits. See Section 13 for timing details.
39	TSYNC	I/O	**Transmit Sync**. A pulse at this pin will establish either frame or CAS multiframe boundaries for the DS2143. Via TCR1.1, the DS2143 can be programmed to output either a frame or multiframe pulse at this pin. See Section 13 for timing details.
40	VDD	-	**Positive Supply.** 5.0 volts.

DS2143 REGISTER MAP

ADDRESS A7 to A0	HEX	R/W	REGISTER NAME
00000000	00	R	Bipolar Violation Count Register 1.
00000001	01	R	Bipolar Violation Count Register 2.
00000010	02	R	CRC4 Count Register 1.
00000011	03	R	CRC4 Count Register 2.
00000100	04	R	E-Bit Count Register 1.
00000101	05	R	E-Bit Count Register 2.
00000110	06	R/W	Status Register 1.
00000111	07	R/W	Status Register 2.
00001000	08	R/W	Receive Information Register.
00011110	1E	R	Synchronizer Status Register.
00010110	16	R/W	Interrupt Mask Register 1.
00010111	17	R/W	Interrupt Mask Register 2.
00010000	10	R/W	Receive Control Register 1.
00010001	11	R/W	Receive Control Register 2.
00010010	12	R/W	Transmit Control Register 1.
00010011	13	R/W	Transmit Control Register 2.
00010100	14	R/W	Common Control Register.
00010101	15	R/W	Test Register.
00011000	18	W	LI Control Register Byte 1.
00011001	19	W	LI Control Register Byte 2.
00100000	20	R/W	Transmit Align Frame Register.
00100001	21	R/W	Transmit Non-Align Frame Register.
00101111	2F	R	Receive Align Frame Register.
00011111	1F	R	Receive Non-Align Frame Register.
00100010	22	R/W	Transmit Channel Blocking Register 1.
00100011	23	R/W	Transmit Channel Blocking Register 2.
00100100	24	R/W	Transmit Channel Blocking Register 3.
00100101	25	R/W	Transmit Channel Blocking Register 4.
00100110	26	R/W	Transmit Idle Register 1.
00100111	27	R/W	Transmit Idle Register 2.
00101000	28	R/W	Transmit Idle Register 3.
00101001	29	R/W	Transmit Idle Register 4.
00101010	2A	R/W	Transmit Idle Definition Register.
00101011	2B	R/W	Receive Channel Blocking Register 1.
00101100	2C	R/W	Receive Channel Blocking Register 2.
00101101	2D	R/W	Receive Channel Blocking Register 3.

ADDRESS A7 to A0	HEX	R/W	REGISTER NAME
00101110	2E	R/W	Receive Channel Blocking Register 4.
00110000	30	R	Receive Signaling Register 1.
00110001	31	R	Receive Signaling Register 2.
00110010	32	R	Receive Signaling Register 3.
00110011	33	R	Receive Signaling Register 4.
00110100	34	R	Receive Signaling Register 5.
00110101	35	R	Receive Signaling Register 6.
00110110	36	R	Receive Signaling Register 7.
00110111	37	R	Receive Signaling Register 8.
00111000	38	R	Receive Signaling Register 9.
00111001	39	R	Receive Signaling Register 10.
00111010	3A	R	Receive Signaling Register 11.
00111011	3B	R	Receive Signaling Register 12.
00111100	3C	R	Receive Signaling Register 13.
00111101	3D	R	Receive Signaling Register 14.
00111110	3E	R	Receive Signaling Register 15.
00111111	3F	R	Receive Signaling Register 16.
01000000	40	R/W	Transmit Signaling Register 1.
01000001	41	R/W	Transmit Signaling Register 2.
01000010	42	R/W	Transmit Signaling Register 3.
01000011	43	R/W	Transmit Signaling Register 4.
01000100	44	R/W	Transmit Signaling Register 5.
01000101	45	R/W	Transmit Signaling Register 6.
01000110	46	R/W	Transmit Signaling Register 7.
01000111	47	R/W	Transmit Signaling Register 8.
01001000	48	R/W	Transmit Signaling Register 9.
01001001	49	R/W	Transmit Signaling Register 10.
01001010	4A	R/W	Transmit Signaling Register 11.
01001011	4B	R/W	Transmit Signaling Register 12.
01001100	4C	R/W	Transmit Signaling Register 13.

ADDRESS A7 to A0	HEX	R/W	REGISTER NAME
01001101	4D	R/W	Transmit Signaling Register 14.
01001110	4E	R/W	Transmit Signaling Register 15.
01001111	4F	R/W	Transmit Signaling Register 16.

Note: All values indicated within the Address column are hexadecimal.

2.0 PARALLEL PORT

The DS2143 is controlled via a multiplexed bidirectional address/data bus by an external microcontroller or microprocessor. The DS2143 can operate with either Intel or Motorola bus timing configurations. If the BTS pin is tied low, Intel timing will be selected; if tied high, Motorola timing will be selected. All Motorola bus signals are listed in parentheses (). See the timing diagrams in the AC Electrical Characteristics for more details. The multiplexed bus on the DS2143 saves pins because the address information and data information share the same signal paths. The addresses are presented to the pins in the first portion of the bus cycle and data will be transferred on the pins during second portion of the bus cycle. Addresses must be valid prior to the falling edge of ALE(AS), at which time the DS2143 latches the address from the AD0 to AD7 pins. Valid write data must be present and held stable during the later portion of the DS or $\overline{WR}$ pulses. In a read cycle, the DS2143 outputs a byte of data during the latter portion of the DS or $\overline{RD}$ pulses. The read cycle is terminated and the bus returns to a high impedance state as $\overline{RD}$ transitions high in Intel timing or as DS transitions low in Motorola timing.

3.0 CONTROL AND TEST REGISTERS

The operation of the DS2143 is configured via a set of five registers. Typically, the control registers are only accessed when the system is first powered up. Once the DS2143 has been initialized, the control registers will only need to be accessed when there is a change in the system configuration. There are two Receive Control Registers (RCR1 and RCR2), two Transmit Control Registers (TCR1 and TCR2), and a Common Control Register (CCR). Each of the five registers is described in this section.

The Test Register at address 15 hex is used by the factory in testing the DS2143. On power-up, the Test Register should be set to 00 hex in order for the DS2143 to operate properly.

RCR1: RECEIVE CONTROL REGISTER 1 (Address=10 Hex)

(MSB)							(LSB)
RSMF	RSM	RSIO	-	-	FRC	SYNCE	RESYNC

SYMBOL	POSITION	NAME AND DESCRIPTION
RSMF	RCR1.7	**RSYNC Multiframe Function**. Only used if the RSYNC pin is programmed in the multiframe mode (RCR1.6=1). 0 = RSYNC outputs CAS multiframe boundaries 1 = RSYNC outputs CRC4 multiframe boundaries
RSM	RCR1.6	**RSYNC Mode Select**. 0 = frame mode (see the timing in Section 13) 1 = multiframe mode (see the timing in Section 13)
RSIO	RCR1.5	**RSYNC I/O Select**. 0 = RSYNC is an output (depends on RCR1.6) 1 = RSYNC is an input (only valid if elastic store enabled) (note: this bit must be set to 0 when RCR2.1=0)
-	RCR1.4	**Not Assigned**. Should be set to 0 when written to.
-	RCR1.3	**Not Assigned**. Should be set to 0 when written to.
FRC	RCR1.2	**Frame Resync Criteria**. 0 = resync if FAS received in error 3 consecutive times 1 = resync if FAS or bit 2 of non-FAS is received in error 3 consecutive times
SYNCE	RCR1.1	**Sync Enable**. 0 = auto resync enabled 1 = auto resync disabled
RESYNC	RCR1.0	**Resync**. When toggled from low to high, a resync is initiated. Must be cleared and set again for a subsequent resync.

SYNC/RESYNC CRITERIA Table 2

FRAME OR MULTIFRAME LEVEL	SYNC CRITERIA	RESYNC CRITERIA	ITU SPEC.
FAS	FAS present in frames N and N + 2, and FAS not present in frame N + 1.	Three consecutive incorrect FAS received. Alternate (RCR1.2=1) the above criteria is met or three consecutive incorrect bit 2 of non-FAS received.	G.706 4.1.1 4.1.2
CRC4	Two valid MF alignment words found within 8 ms.	915 or more CRC4 code words out of 1000 received in error.	G.706 4.2 4.3.2
CAS	Valid MF alignment word found and previous time slot 16 contains code other than all 0s.	Two consecutive MF alignment words received in error.	G.732 5.2

RCR2: RECEIVE CONTROL REGISTER 2 (Address=11 Hex)

(MSB)							(LSB)
Sa8S	Sa7S	Sa6S	Sa5S	Sa4S	SCLKM	ESE	-

SYMBOL	POSITION	NAME AND DESCRIPTION
Sa8S	RCR2.7	**Sa8 Bit Select**. Set to 1 to report the Sa8 bit at the RLINK pin; set to 0 to not report the Sa8 bit.
Sa7S	RCR2.6	**Sa7 Bit Select**. Set to 1 to report the Sa7 bit at the RLINK pin; set to 0 to not report the Sa7 bit.
Sa6S	RCR2.5	**Sa6 Bit Select**. Set to 1 to report the Sa6 bit at the RLINK pin; set to 0 to not report the Sa6 bit.
Sa5S	RCR2.4	**Sa5 Bit Select**. Set to 1 to report the Sa5 bit at the RLINK pin; set to 0 to not report the Sa5 bit.
Sa4S	RCR2.3	**Sa4 Bit Select**. Set to 1 to report the Sa4 bit at the RLINK pin; set to 0 to not report the Sa4 bit.
SCLKM	RCR2.2	**SYSCLK Mode Select**. 0 = if SYSCLK is 1.544 MHz. 1 = if SYSCLK is 2.048 MHz.
ESE	RCR2.1	**Elastic Store Enable**. 0 = elastic store is bypassed. 1 = elastic store is enabled.
-	RCR2.0	**Not Assigned**. Should be set to 0 when written to.

TCR1: TRANSMIT CONTROL REGISTER 1 (Address=12 Hex)

(MSB)							(LSB)
ODF	TFPT	T16S	TUA1	TSiS	TSA1	TSM	TSIO

SYMBOL	POSITION	NAME AND DESCRIPTION
ODF	TCR1.7	**Output Data Format**. 0 = bipolar data at TPOS and TNEG. 1 = NRZ data at TPOS; TNEG=0.
TFPT	TCR1.6	**Transmit Timeslot 0 Pass Through**. 0 = FAS bits/Sa bits/Remote Alarm sourced internally from the TAF and TNAF registers. 1 = FAS bits/Sa bits/Remote Alarm sourced from TSER.
T16S	TCR1.5	**Transmit Timeslot 16 Data Select**. 0 = sample timeslot 16 at TSER pin. 1 = source timeslot 16 from TS1 to TS16 registers.
TUA1	TCR1.4	**Transmit Unframed All 1s**. 0 = transmit data normally. 1 = transmit an unframed all 1s code at TPOS and TNEG.
TSiS	TCR1.3	**Transmit International Bit Select**. 0 = sample Si bits at TSER pin. 1 = source Si bits from TAF and TNAF registers (in this mode, TCR1.6 must be set to 0).
TSA1	TCR1.2	**Transmit Signaling All 1s**. 0 = normal operation. 1 = force timeslot 16 in every frame to all 1s.
TSM	TCR1.1	**TSYNC Mode Select**. 0 = frame mode (see the timing in Section 13). 1 = CAS and CRC4 multiframe mode (see the timing in Section 13).
TSIO	TCR1.0	**TSYNC I/O Select**. 0 = TSYNC is an input. 1 = TSYNC is an output.

TCR2: TRANSMIT CONTROL REGISTER 2 (Address=13 Hex)

(MSB)							(LSB)
Sa8S	Sa7S	Sa6S	Sa5S	Sa4S	-	AEBE	P34F

SYMBOL	POSITION	NAME AND DESCRIPTION
Sa8S	TCR2.7	**Sa8 Bit Select**. Set to 1 to source the Sa8 bit from the TLINK pin; set to 0 to not source the Sa8 bit.
Sa7S	TCR2.6	**Sa7 Bit Select**. Set to 1 to source the Sa7 bit from the TLINK pin; set to 0 to not source the Sa7 bit.
Sa6S	TCR2.5	**Sa6 Bit Select**. Set to 1 to source the Sa6 bit from the TLINK pin; set to 0 to not source the Sa6 bit.
Sa5S	TCR2.4	**Sa5 Bit Select**. Set to 1 to source the Sa5 bit from the TLINK pin; set to 0 to not source the Sa5 bit.
Sa4S	TCR2.3	**Sa4 Bit Select**. Set to 1 to source the Sa4 bit from the TLINK pin; set to 0 to not source the Sa4 bit.
-	TCR2.2	**Not Assigned**. Should be set to 0 when written to.
AEBE	TCR2.1	**Automatic E-Bit Enable**. 0 = E-bits not automatically set in the transmit direction. 1 = E-bits automatically set in the transmit direction.
P34F	TCR2.0	**Function of Pin 34**. 0 = Receive Loss of Sync (RLOS). 1 = Loss of Transmit Clock (LOTC).

CCR: COMMON CONTROL REGISTER (Address=14 Hex)

(MSB)							(LSB)
LLB	THDB3	TG802	TCRC4	RSM	RHDB3	RG802	RCRC4

SYMBOL	POSITION	NAME AND DESCRIPTION
LLB	CCR.7	**Local Loopback**. 0 = loopback disabled. 1 = loopback enabled.
THDB3	CCR.6	**Transmit HDB3 Enable**. 0 = HDB3 disabled. 1 = HDB3 enabled.
TG802	CCR.5	**Transmit G.802 Enable**. See Section 13 for details. 0 = do not force TCHBLK high during bit 1 of timeslot 26. 1 = force TCHBLK high during bit 1 of timeslot 26.
TCRC4	CCR.4	**Transmit CRC4 Enable**. 0 = CRC4 disabled. 1 = CRC4 enabled.
RSM	CCR.3	**Receive Signaling Mode Select**. 0 = CAS signaling mode. 1 = CCS signaling mode.
RHDB3	CCR.2	**Receive HDB3 Enable**. 0 = HDB3 disabled. 1 = HDB3 enabled.
RG802	CCR.1	**Receive G.802 Enable**. See Section 13 for details. 0 = do not force RCHBLK high during bit 1 of timeslot 26 1 = force RCHBLK high during bit 1 of timeslot 26.
RCRC4	CCR.0	**Receive CRC4 Enable**. 0 = CRC4 disabled. 1 = CRC4 enabled.

LOCAL LOOPBACK

When CCR.7 is set to a 1, the DS2143 will enter a Local LoopBack (LLB) mode. This loopback is useful in testing and debugging applications. In LLB, the DS2143 will loop data from the transmit side back to the receive side. This loopback is synonymous with replacing the RCLK input with the TCLK signal, and the RPOS/RNEG inputs with the TPOS/TNEG outputs. When LLB is enabled, the following will occur:

1. data at RPOS and RNEG will be ignored;
2. all receive side signals will take on timing synchronous with TCLK instead of RCLK;
3. all functions are available.

4.0 STATUS AND INFORMATION REGISTERS

There is a set of four registers that contain information on the current real time status of the DS2143: Status Register 1 (SR1), Status Register 2 (SR2), Receive Information Register (RIR), and Synchronizer Status Register (SSR). When a particular event has occurred (or is occurring), the appropriate bit in one of these three registers will be set to a 1. All of the bits in these registers operate in a latched fashion (except for the SSR). This means that if an event occurs and a bit is set to a 1 in any of the registers, it will remain set until the user reads that bit. The bit will be cleared when it is read and it will not be set again until the event has occurred again or if the alarm(s) is still present.

The user will always precede a read of the SR1, SR2, and RIR registers with a write. The byte written to the register will inform the DS2143 which bits the user wishes to read and have cleared. The user will write a byte to one of these three registers, with a 1 in the bit positions he or she wishes to read and a 0 in the bit positions he or she does not wish to obtain the latest information on. When a 1 is written to a bit location, the read register will be updated with current value and it will be cleared. When a 0 is written to a bit position, the read register will not be updated and the previous value will be held. A write to the status and information registers will be immediately followed by a read of the same register. The read result should be logically AND'ed with the mask byte that was just written and this value should be written back into the same register to insure that the bit does indeed clear. This second write is necessary because the alarms and events in the status registers occur asynchronously in respect to their access via the parallel port. This scheme allows an external microcontroller or microprocessor to individually poll certain bits without disturbing the other bits in the register. This operation is key in controlling the DS2143 with higher order software languages.

The SSR register operates differently than the other three. It is a read only register and it reports the status of the synchronizer in real time. This register is not latched and it is not necessary to precede a read of this register with a write.

The SR1 and SR2 registers have the unique ability to initiate a hardware interrupt via the $\overline{\text{INT1}}$ and $\overline{\text{INT2}}$ pins respectively. Each of the alarms and events in the SR1 and SR2 can be either masked or unmasked from the interrupt pins via the Interrupt Mask Register 1 (IMR1) and Interrupt Mask Register 2 (IMR2) respectively.

RIR: RECEIVE INFORMATION REGISTER (Address=08 Hex)

(MSB)							(LSB)
-	-	-	ESF	ESE	-	FASRC	CASRC

SYMBOL	POSITION	NAME AND DESCRIPTION
-	RIR.7	**Not Assigned**. Could be any value when read.
-	RIR.6	**Not Assigned**. Could be any value when read.
-	RIR.5	**Not Assigned**. Could be any value when read.
ESF	RIR.4	**Elastic Store Full**. Set when the elastic store buffer fills and a frame is deleted.
ESE	RIR.3	**Elastic Store Empty**. Set when the elastic store buffer empties and a frame is repeated.
-	RIR.2	**Not Assigned**. Could be any value when read.
FASRC	RIR.1	**FAS Resync Criteria Met**. Set when three consecutive FAS words are received in error.
CASRC	RIR.0	**CAS Resync Criteria Met**. Set when two consecutive CAS MF alignment words are received in error.

SSR: SYNCHRONIZER STATUS REGISTER (Address=1E Hex)

(MSB)							(LSB)
CSC5	CSC4	CSC3	CSC2	CSC0	FASSA	CASSA	CRC4SA

SYMBOL	POSITION	NAME AND DESCRIPTION
CSC5	SSR.7	**CRC4 Sync Counter Bit 5**. MSB of the 6-bit counter.
CSC4	SSR.6	**CRC4 Sync Counter Bit 4**.
CSC3	SSR.5	**CRC4 Sync Counter Bit 3**.
CSC2	SSR.4	**CRC4 Sync Counter Bit 2**.
CSC1	SSR.3	**CRC4 Sync Counter Bit 0**. LSB of the 6-bit counter. The next to LSB is not accessible.
FASSA	SSR.2	**FAS Sync Active**. Set while the synchronizer is searching for alignment at the FAS level.
CASSA	SSR.1	**CAS MF Sync Active**. Set while the synchronizer is searching for the CAS MF alignment word.
CRC4SA	SSR.0	**CRC4 MF Sync Active**. Set while the synchronizer is searching for the CRC4 MF alignment word.

CRC4 SYNC COUNTER

The CRC4 Sync Counter increments each time the 8ms CRC4 multiframe search times out. The counter is cleared when the DS2143 has successfully obtained synchronization at the CRC4 level. The counter can also be cleared by disabling the CRC4 mode (CCR.0=0). This counter is useful for determining the amount of time the DS2143 has been searching for synchronization at the CRC4 level. Annex B of CCITT G.706 suggests that if synchronization at the CRC4 level cannot be obtained within 400 ms, then the search should be abandoned and proper action taken. The CRC4 Sync Counter will rollover

SR1: STATUS REGISTER 1 (Address=06 Hex)

(MSB)							(LSB)
RSA1	RDMA	RSA0	SLIP	RUA1	RRA	RCL	RLOS

SYMBOL	POSITION	NAME AND DESCRIPTION
RSA1	SR1.7	**Receive Signaling All 1s**. Set when the contents of timeslot 16 contains less than 3 0s over 16 consecutive frames. This alarm is not disabled in the CCS signaling mode.
RDMA	SR1.6	**Receive Distant MF Alarm**. Set when bit 6 of timeslot 16 in frame 0 has been set for 2 consecutive multiframes. This alarm is not disabled in the CCS signaling mode.
RSA0	SR1.5	**Receive Signaling All 0s**. Set when over a full MF, timeslot 16 contains all 0s.
SLIP	SR1.4	**Elastic Store Slip Occurrence**. Set when the elastic store has either repeated or deleted a frame of data.
RUA1	SR1.3	**Receive Unframed All 1s**. Set when an unframed all 1s code is received at RPOS and RNEG.
RRA	SR1.2	**Receive Remote Alarm**. Set when a remote alarm is received at RPOS and RNEG.
RCL	SR1.1	**Receive Carrier Loss**. Set when 255 consecutive 0s have been detected at RPOS and RNEG.
RLOS	SR1.0	**Receive Loss of Sync**. Set when the device is not synchronized to the receive E1 stream.

ALARM CRITERIA Table 2

ALARM	SET CRITERIA	CLEAR CRITERIA	ITU SPEC.
RSA1 (receive signaling all 1s)	over 16 consecutive frames (one full MF) timeslot 16 contains less than 3 0s	over 16 consecutive frames (one full MF) timeslot 16 contains three or more 0s	G.732 4.2
RSA0 (receive signaling all 0s)	over 16 consecutive frames (one full MF) timeslot 16 contains all 0s	over 16 consecutive frames (one full MF) timeslot 16 contains at least a single 1	G.732 5.2
RDMA (receive distant multiframe alarm)	bit 6 in timeslot 16 of frame 0 set to 1 for two consecutive MFs	bit 6 in timeslot 16 of frame 0 set to 0 for two consecutive MFs	O.162 2.1.5
RUA1 (receive unframed all 1s)	less than three 0s in two frames (512 bits)	more than two 0s in two frames (512 bits)	O.162 1.6.1.2
RRA (receive remote alarm)	bit 3 of non-align frame set to 1 for three consecutive occasions	bit 3 of non-align frame set to 0 for three consecutive occasions	O.162 2.1.4
RCL (receive carrier loss)	255 consecutive 0s received	in 255 bit times, at least 32 1s are received	G.775

Note: all the alarm bits in Status Register 1 except the RUA1 will remain set after they are read if the alarm condition still exists; the RUA1 will clear and check the next 512 bits for an all 1s condition at which point it will again be set if the alarm condition still is present.

SR2: STATUS REGISTER 2 (Address=07 Hex)

(MSB)							(LSB)
RMF	RAF	TMF	SEC	TAF	LOTC	RCMF	LORC

SYMBOL	POSITION	NAME AND DESCRIPTION
RMF	SR2.7	**Receive CAS Multiframe**. Set every 2 ms (regardless if CAS signaling is enabled or not) on receive multiframe boundaries. Used to alert the host that signaling data is available.
RAF	SR2.6	**Receive Align Frame**. Set every 250 µs at the beginning of align frames. Used to alert the host that Si and Sa bits are available in the RAF and RNAF registers.
TMF	SR2.5	**Transmit Multiframe**. Set every 2 ms (regardless if CRC4 is enabled) on transmit multiframe boundaries. Used to alert the host that signaling data needs to be updated.
SEC	SR2.4	**One-Second Timer**. Set on increments of 1 second based on RCLK.
TAF	SR2.3	**Transmit Align Frame**. Set every 250 µs at the beginning of align frames. Used to alert the host that the TAF and TNAF registers need to be updated.
LOTC	SR2.2	**Loss of Transmit Clock**. Set when the TCLK pin has not transitioned for one channel time (or 3.9 µs). Will force pin 34 high if enabled via TCR2.0. Based on RCLK.
RCMF	SR2.1	**Receive CRC4 Multiframe**. Set on CRC4 multiframe boundaries; will continue to be set every 2 ms on an arbitrary boundary if CRC4 is disabled.
LORC	SR2.0	**Loss of Receive Clock**. Set when the RCLK pin has not transitioned for at least 2 µs (3 µs ±1 µs).

IMR1: INTERRUPT MASK REGISTER 1 (Address=16 Hex)

(MSB)							(LSB)
RSA1	RDMA	RSA0	SLIP	RUA1	RRA	RCL	RLOS

SYMBOL	POSITION	NAME AND DESCRIPTION
RSA1	IMR1.7	**Receive Signaling All 1s**. 0 = interrupt masked. 1 = interrupt enabled.
RDMA	IMR1.6	**Receive Distant MF Alarm**. 0 = interrupt masked. 1 = interrupt enabled.
RSA0	IMR1.5	**Receive Signaling All 0s**. 0 = interrupt masked. 1 = interrupt enabled.
SLIP	IMR1.4	**Elastic Store Slip Occurrence**. 0 = interrupt masked. 1 = interrupt enabled.
RUA1	IMR1.3	**Receive Unframed All 1s**. 0 = interrupt masked. 1 = interrupt enabled.
RRA	IMR1.2	**Receive Remote Alarm**. 0 = interrupt masked. 1 = interrupt enabled.
RCL	IMR1.1	**Receive Carrier Loss**. 0 = interrupt masked. 1 = interrupt enabled.
RLOS	IMR1.0	**Receive Loss of Sync**. 0 = interrupt masked. 1 = interrupt enabled.

IMR2: INTERRUPT MASK REGISTER 2 (Address=17 Hex)

(MSB)							(LSB)
RMF	RAF	TMF	SEC	TAF	LOTC	RCMF	LORC

SYMBOL	POSITION	NAME AND DESCRIPTION
RMF	IMR2.7	**Receive CAS Multiframe**. 0 = interrupt masked. 1 = interrupt enabled.
RAF	IMR2.6	**Receive Align Frame**. 0 = interrupt masked. 1 = interrupt enabled.
TMF	IMR2.5	**Transmit Multiframe**. 0 = interrupt masked. 1 = interrupt enabled.
SEC	IMR2.4	**1-Second Timer**. 0 = interrupt masked. 1 = interrupt enabled.
TAF	IMR2.3	**Transmit Align Frame**. 0 = interrupt masked. 1 = interrupt enabled.
LOTC	IMR2.2	**Loss Of Transmit Clock**. 0 = interrupt masked. 1 = interrupt enabled.
RCMF	IMR2.1	**Receive CRC4 Multiframe**. 0 = interrupt masked. 1 = interrupt enabled.
LORC	IMR2.0	**Loss of Receive Clock**. 0 = interrupt masked. 1 = interrupt enabled.

5.0 ERROR COUNT REGISTERS

There are a set of three counters in the DS2143 that record bipolar violations, errors in the CRC4 SMF code words, and E-bits as reported by the far end. Each of these three counters are automatically updated on 1-second boundaries as determined by the 1-second timer in Status Register 2 (SR2.4). Hence, these registers contain performance data from the previous second. The user can use the interrupt from the 1-second timer to determine when to read these registers. The user has a full second to read the counters before the data is lost.

BPVCR1:
UPPER BIPOLAR VIOLATION COUNT REGISTER 1 (Address=00 Hex)
BPVCR2:
LOWER BIPOLAR VIOLATION COUNT REGISTER 2 (Address=01 Hex)

(MSB)							(LSB)	
BV7	BV6	BV5	BV4	BV3	BV2	BV1	BV0	BPVCR2
BV15	BV14	BV13	BV12	BV11	BV10	BV9	BV8	BPVCR1

SYMBOL	POSITION	NAME AND DESCRIPTION
BV15	BPVCR1.7	MSB of the bipolar violation count.
BV0	BPVCR2.0	LSB of the bipolar violation count.

Bipolar Violation Count Register 1 (BPVCR1) is the most significant word and BPVCR2 is the least significant word of a 16-bit counter that records bipolar violations (BPVs). If the HDB3 mode is set for the receive side via CCR.2, then HDB3 code words are not counted. This counter increments at all times and is not disabled by loss of sync conditions. The counter saturates at 65,535 and will not rollover. The bit error rate on a E1 line would have to be greater than 10**-2 before the BPVCR would saturate.

CRCCR1: CRC4 COUNT REGISTER 1 (Address=02 Hex)
CRCCR2: CRC4 COUNT REGISTER 2 (Address=03 Hex)

(MSB)							(LSB)	
CRC7	CRC6	CRC5	CRC4	CRC3	CRC2	CRC1	CRC0	CRCCR2
CRC14	CRC14	CRC13	CRC12	CRC11	CRC10	CRC9	CRC8	CRCCR1

SYMBOL	POSITION	NAME AND DESCRIPTION
CRC15	CRCCR1.7	MSB of the CRC4 error count.
CRC0	CRCCR2.0	LSB of the CRC4 error count.

CRC4 Count Register 1 (CRCCR1) is the most significant word and CRCCR2 is the least significant word of a 16-bit counter that records word errors in the Cyclic Redundancy Check 4 (CRC4). Since the maximum CRC4 count in a 1-second period is 1000, this counter cannot saturate. The counter is disabled during loss of sync at either the FAS or CRC4 level; it will continue to count if loss of sync occurs at the CAS level.

EBCR1: E-BIT COUNT REGISTER 1 (Address=04 Hex)
EBCR2: E-BIT COUNT REGISTER 2 (Address=05 Hex)

(MSB)							(LSB)	
EB7	EB6	EB5	EB4	EB3	EB2	EB1	EB0	EBCR2
EB15	EB14	EB13	EB12	EB11	EB10	EB9	EB8	EBCR1

SYMBOL	POSITION	NAME AND DESCRIPTION
EB15	EBCR1.7	MSB of the E-Bit error count.
EB0	EBCR2.0	LSB of the E-Bit error count.

E-bit Count Register 1 (EBCR1) is the most significant word and EBCR2 is the least significant word of a 16-bit counter that records Far End Block Errors (FEBE) as reported in the first bit of frames 13 and 15 on E1 lines running with CRC4 multiframe. These count registers will increment once each time the received E-bit is set to 0. Since the maximum E-bit count in a 1-second period is 1000, this counter cannot saturate. The counter is disabled during loss of sync at either the FAS or CRC4 level; it will continue to count if loss of sync occurs at the CAS level.

6.0 Sa DATA LINK CONTROL AND OPERATION

The DS2143 provides for access to the proposed E1 performance monitor data link in the Sa bit positions. The device allows access to the Sa bits either via a set of two internal registers (RNAF and TNAF) or via two external pins (RLINK and TLINK).

On the receive side, the Sa bits are always reported in the internal RNAF register (see Section 11 for more details). All five Sa bits are always output at the RLINK pin. See Section 13 for detailed timing. Via RCR2, the user can control the RLCLK pin to pulse during any combination of Sa bits. This allows the user to create a clock that can be used to capture the needed Sa bits.

On the transmit side, the individual Sa bits can be either sourced from the internal TNAF register (TCR1.6=0) or from the external TLINK pin. Via TCR2, the DS2143 can be programmed to source any combination of the additional bits from the TLINK pin. If the user wishes to pass the Sa bits through the DS2143 without them being altered, then the device should be set up to source all 5 Sa bits via the TLINK pin and the TLINK pin should be tied to the TSER pin. Please see the timing diagrams and the transmit data flow diagram in Section 13 for examples.

7.0 SIGNALING OPERATION

The Channel Associated Signaling (CAS) bits embedded in the E1 stream can be extracted from the receive stream and inserted into the transmit stream by the DS2143. Each of the 30 channels has 4 signaling bits (A/B/C/D) associated with it. The numbers in parenthesis () are the channel associated with a particular signaling bit. The channel numbers have been assigned as described in the CCITT documents. For example, channel 1 is associated with timeslot 1 and channel 30 is associated with timeslot 31. There is a set of 16 registers for the receive side (RS1 to RS16) and 16 registers on the transmit side (TS1 to TS16). The signaling registers are detailed below.

RS1 TO RS16: RECEIVE SIGNALING REGISTERS (Address=30 to 3F Hex)

(MSB)							(LSB)	
0	**0**	**0**	**0**	**X**	**Y**	**X**	**X**	RS1 (30)
A(1)	B(1)	C(1)	D(1)	A(16)	B(16)	C(16)	D(16)	RS2 (31)
A(2)	B(2)	C(2)	D(2)	A(17)	B(17)	C(17)	D(17)	RS3 (32)
A(3)	B(3)	C(3)	D(3)	A(18)	B(18)	C(18)	D(18)	RS4 (33)
A(4)	B(4)	C(4)	D(4)	A(19)	B(19)	C(19)	D(19)	RS5 (34)
A(5)	B(5)	C(5)	D(5)	A(20)	B(20)	C(20)	D(20)	RS6 (35)
A(6)	B(6)	C(6)	D(6)	A(21)	B(21)	C(21)	D(21)	RS7 (36)
A(7)	B(7)	C(7)	D(7)	A(22)	B(22)	C(22)	D(22)	RS8 (37)
A(8)	B(8)	C(8)	D(8)	A(23)	B(23)	C(23)	D(23)	RS9 (38)
A(9)	B(9)	C(9)	D(9)	A(24)	B(24)	C(24)	D(24)	RS10 (39)
A(10)	B(10)	C(10)	D(10)	A(25)	B(25)	C(25)	D(25)	RS11 (3A)
A(11)	B(11)	C(11)	D(11)	A(26)	B(26)	C(26)	D(26)	RS12 (3B)
A(12)	B(12)	C(12)	D(12)	A(27)	B(27)	C(27)	D(27)	RS13 (3C)
A(13)	B(13)	C(13)	D(13)	A(28)	B(28)	C(28)	D(28)	RS14 (3D)
A(14)	B(14)	C(14)	D(14)	A(29)	B(29)	C(29)	D(29)	RS15 (3E)
A(15)	B(15)	C(15)	D(15)	A(30)	B(30)	C(30)	D(30)	RS16 (3F)

SYMBOL	POSITION	NAME AND DESCRIPTION
X	RS1.0/1/3	Spare Bits.
Y	RS1.2	Remote Alarm Bit (integrated and reported in SR1.6).
A(1)	RS2.7	Signaling Bit A for Channel 1.
D(30)	RS16.0	Signaling Bit D for Channel 30.

Each Receive Signaling Register (RS1 to RS16) reports the incoming signaling from two timeslots. The bits in the Receive Signaling Registers are updated on multiframe boundaries so the user can utilize the Receive Multiframe Interrupt in the Receive Status Register 2 (SR2.7) to know when to retrieve the signaling bits. The user has a full 2 ms to retrieve the signaling bits before the data is lost. The RS registers are updated under all conditions. Their validity should be qualified by checking for synchronization at the CAS level. In CCS signaling mode, RS1 to RS16 can also be used to extract signaling information. Via the SR2.7 bit, the user will be informed when the signaling registers have been loaded with data. The user has 2 ms to retrieve the data before it is lost.

TS1 TO TS16: TRANSMIT SIGNALING REGISTERS (Address=40 to 4F Hex)

(MSB)							(LSB)	
0	**0**	**0**	**0**	**X**	**Y**	**X**	**X**	TS1 (40)
A(1)	B(1)	C(1)	D(1)	A(16)	B(16)	C(16)	D(16)	TS2 (41)
A(2)	B(2)	C(2)	D(2)	A(17)	B(17)	C(17)	D(17)	TS3(42)
A(3)	B(3)	C(3)	D(3)	A(18)	B(18)	C(18)	D(18)	TS4 (43)
A(4)	B(4)	C(4)	D(4)	A(19)	B(19)	C(19)	D(19)	TS5 (44)
A(5)	B(5)	C(5)	D(5)	A(20)	B(20)	C(20)	D(20)	TS6 (45)
A(6)	B(6)	C(6)	D(6)	A(21)	B(21)	C(21)	D(21)	TS7 (46)
A(7)	B(7)	C(7)	D(7)	A(22)	B(22)	C(22)	D(22)	TS8 (47)
A(8)	B(8)	C(8)	D(8)	A(23)	B(23)	C(23)	D(23)	TS9 (48)
A(9)	B(9)	C(9)	D(9)	A(24)	B(24)	C(24)	D(24)	TS10 (49)
A(10)	B(10)	C(10)	D(10)	A(25)	B(25)	C(25)	D(25)	TS11 (4A)
A(11)	B(11)	C(11)	D(11)	A(26)	B(26)	C(26)	D(26)	TS12 (4B)
A(12)	B(12)	C(12)	D(12)	A(27)	B(27)	C(27)	D(27)	TS13(4C)
A(13)	B(13)	C(13)	D(13)	A(28)	B(28)	C(28)	D(28)	TS14 (4D)
A(14)	B(14)	C(14)	D(14)	A(29)	B(29)	C(29)	D(29)	TS15 (4E)
A(15)	B(15)	C(15)	D(15)	A(30)	B(30)	C(30)	D(30)	TS16 (4F)

SYMBOL	POSITION	NAME AND DESCRIPTION
X	TS1.0/1/3	Spare Bits.
Y	TS1.2	Remote Alarm Bit.
A(1)	TS2.7	Signaling Bit A for Channel 1.
D(30)	TS16.0	Signaling Bit D for Channel 30.

Each Transmit Signaling Register (TS1 to TS16) contains the CAS bits for two timeslots that will be inserted into the outgoing stream if enabled to do so via TCR1.5. On multiframe boundaries, the DS2143 will load the values present in the Transmit Signaling Register into an outgoing signaling shift register that is internal to the device. The user can utilize the Transmit Multiframe bit in Status Register 2 (SR2.5) to know when to update the signaling bits. The bit will be set every 2 ms and the user has 2 ms to update the TSRs before the old data will be retransmitted.

The TS1 register is special because it contains the CAS multiframe alignment word in its upper nibble. The upper 4 bits must always be set to 0000 or else the terminal at the far end will lose multiframe synchronization. If the user wishes to transmit a multiframe alarm to the far end, then the TS1.2 bit should be set to a 1. If no alarm is to be transmitted, then the TS1.2 bit should be cleared. The three remaining bits in TS1 are the spare bits. If they are not used, they should be set to 1. In CCS signaling mode, TS1 to TS16 can also be used to insert signaling information. Via the SR2.5 bit, the user will be informed when the signaling registers need to be loaded with data. The user has 2 ms to load the data before the old data will be retransmitted.

8.0 TRANSMIT IDLE REGISTERS

There is a set of five registers in the DS2143 that can be used to custom tailor the data that is to be transmitted onto the E1 line, on a channel by channel basis. Each of the 32 E1 channels can be forced to have a user defined idle code inserted into them.

TIR1/TIR2/TIR3/TIR4: TRANSMIT IDLE REGISTERS (Address=26 to 29 Hex)

(MSB)							(LSB)	
CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	TIR1 (26)
CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	TIR2 (27)
CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	TIR3 (28)
CH32	CH31	CH30	CH29	CH28	CH27	CH26	CH25	TIR4 (29)

SYMBOL	POSITION	NAME AND DESCRIPTION
CH32	TIR4.7	**Transmit Idle Registers.** 0 = do not insert the Idle Code into this channel.
CH1	TIR1.0	1 = insert the Idle Code into this channel.

TIDR: TRANSMIT IDLE DEFINITION REGISTER (Address=2A Hex)

(MSB)							(LSB)
TIDR7	TIDR6	TIDR5	TIDR4	TIDR3	TIDR2	TIDR1	TIDR0

SYMBOL	POSITION	NAME AND DESCRIPTION
TIDR7	TIDR.7	MSB of the Idle Code.
TIDR0	TIDR.0	LSB of the Idle Code.

Each of the bit positions in the Transmit Idle Registers (TIR1/TIR2/TIR3/TIR4) represents a timeslot in the outgoing frame. When these bits are set to a 1, the corresponding channel will transmit the Idle Code contained in the Transmit Idle Definition Register (TIDR). In the TIDR, the MSB is transmitted first.

9.0 CLOCK BLOCKING REGISTERS

The Receive Channel Blocking Registers (RCBR1/RCBR2/RCBR3/RCBR4) and the Transmit Channel Blocking Registers (TCBR1/TCBR2/TCBR3/TCBR4) control the RCHBLK and TCHBLK pins respectively. The RCHBLK and TCHCLK pins are user-programmable outputs that can be forced either high or low during individual channels. These outputs can be used to block clocks to a USART or LAPD controller in ISDN-PRI applications. When the appropriate bits are set to a 1, the RCHBLK and TCHCLK pins will be held high during the entire corresponding channel time. See the timing in Section 13 for an example.

RCBR1/RCBR2/RCBR3/RCBR4: RECEIVE CHANNEL BLOCKING REGISTERS (Address=2B to 2E Hex)

(MSB)							(LSB)	
CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	RCBR1 (2B)
CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	RCBR2 (2C)
CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	RCBR3 (2D)
CH32	CH31	CH30	CH29	CH28	CH27	CH26	CH25	RCBR4 (2E)

SYMBOL	POSITION	NAME AND DESCRIPTION
CH32	RCBR4.7	**Receive Channel Blocking Registers.** 0 = force the RCHBLK pin to remain low during this channel time.
CH1	RCBR1.0	1 = force the RCHBLK pin high during this channel time.

TCBR1/TCBR2/TCBR3/TCBR4: TRANSMIT CHANNEL BLOCKING REGISTERS (Address=22 to 25 Hex)

(MSB)							(LSB)	
CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	TCBR1 (22)
CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	TCBR2 (23)
CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	TCBR3 (24)
CH32	CH31	CH30	CH29	CH28	CH27	CH26	CH25	TCBR4 (25)

SYMBOL	POSITION	NAME AND DESCRIPTION
CH32	TCBR4.7	**Receive Channel Blocking Registers.** 0 = force the TCHBLK pin to remain low during this channel time.
CH1	TCBR1.0	1 = force the TCHBLK pin high during this channel time.

10.0 ELASTIC STORE OPERATION

The DS2143 has an onboard two-frame (512 bits) elastic store. This elastic store can be enabled via RCR2.1. If the elastic store is enabled (RCR2.1=1), then the user must provide either a 1.544 MHz (RCR2.2=0) or 2.048 MHz (RCR2.2=1) clock at the SYSCLK pin. If the elastic store is enabled, then the user has the option of either providing a frame sync at the RFSYNC pin (RCR1.5=1) or having the RFSYNC pin provide a pulse on frame or multiframe boundaries (RCR1.5=0). If the user wishes to obtain pulses at the frame boundary, then RCR1.6 must be set to 0, and if the user wishes to have pulses occur at the multiframe boundary, then RCR1.6 must be set to 1. If the user selects to apply a 1.544 MHz clock to the SYSCLK pin, then every fourth channel will be deleted and the F-bit position inserted (forced to 1). Hence channels 1, 5, 9, 13, 17, 21, 25, and 29 (timeslots 0, 4, 8, 12, 16, 20, 24, and 28) will be deleted. Also, in 1.544 MHz applications, the RCHBLK output will not be active in channels 25 through 32 (or in other words, RCBR4 is not active). See Section 13 for more details. If the 512-bit elastic buffer either fills or empties, a controlled slip will occur. If the buffer empties, then a full frame of data (256 bits) will be repeated at RSER and the SR1.4 and RIR.3 bits will be set to a 1. If the buffer fills, then a full frame of data will be deleted and the SR1.4 and RIR.4 bits will be set to a 1.

11.0 ADDITIONAL (Sa) AND INTERNATIONAL (Si) BIT OPERATION

The DS2143 provides for access to both the Additional (Sa) and International (Si) bits. On the receive side, the RAF and RNAF registers will always report the data as it received in the Additional and International bit locations. The RAF and RNAF registers are updated with the setting of the Receive Align Frame bit in Status Register 2 (SR2.6). The host can use the SR2.6 bit to know when to read the RAF and RNAF registers. It has 250 µs to retrieve the data before it is lost.

On the transmit side, data is sampled from the TAF and TNAF registers with the setting of the Transmit Align Frame bit in Status Register 2 (SR2.3). The host can use the SR2.3 bit to know when to update the TAF and TNAF registers. It has 250 µs to update the data or else the old data will be retransmitted. Data in the Si bit position will be overwritten if either the DS2143 is programmed: (1) to source the Si bits from the TSER pin, (2) in the CRC4 mode, or (3) have automatic E-bit insertion enabled. Data in the Sa bit position will be overwritten if any of the TCR2.3 to TCR2.7 bits is set to 1. Please see the register descriptions for TCR1 and TCR2 and the Transmit Data Flow diagram in Section 13 for more details.

RAF: RECEIVE ALIGN FRAME REGISTER (Address=2F Hex)

(MSB)							(LSB)
Si	0	0	1	1	0	1	1

SYMBOL	POSITION	NAME AND DESCRIPTION
Si	RAF.7	International Bit.
0	RAF.6	Frame Alignment Signal Bit.
0	RAF.5	Frame Alignment Signal Bit.
1	RAF.4	Frame Alignment Signal Bit.
1	RAF.3	Frame Alignment Signal Bit.
0	RAF.2	Frame Alignment Signal Bit.
1	RAF.1	Frame Alignment Signal Bit.
1	RAF.0	Frame Alignment Signal Bit.

RNAF: RECEIVE NON-ALIGN FRAME REGISTER (Address=1F Hex)

(MSB)							(LSB)
Si	1	A	Sa4	Sa5	Sa6	Sa7	Sa8

SYMBOL	POSITION	NAME AND DESCRIPTION
Si	RNAF.7	International Bit.
1	RNAF.6	Frame Non-Alignment Signal Bit.
A	RNAF.5	Remote Alarm.
Sa4	RNAF.4	Additional Bit 4.
Sa5	RNAF.3	Additional Bit 5.
Sa6	RNAF.2	Additional Bit 6.
Sa7	RNAF.1	Additional Bit 7.
Sa8	RNAF.0	Additional Bit 8.

TAF: TRANSMIT ALIGN FRAME REGISTER (Address=20 Hex)

(MSB)							(LSB)
Si	0	0	1	1	0	1	1

SYMBOL	POSITION	NAME AND DESCRIPTION
Si	TAF.7	International Bit.
0	TAF.6	Frame Alignment Signal Bit.
0	TAF.5	Frame Alignment Signal Bit.
1	TAF.4	Frame Alignment Signal Bit.
1	TAF.3	Frame Alignment Signal Bit.
0	TAF.2	Frame Alignment Signal Bit.
1	TAF.1	Frame Alignment Signal Bit.
1	TAF.0	Frame Alignment Signal Bit.

TNAF: TRANSMIT NON-ALIGN FRAME REGISTER (Address=21 Hex)

(MSB)							(LSB)
Si	1	A	Sa4	Sa5	Sa6	Sa7	Sa8

SYMBOL	POSITION	NAME AND DESCRIPTION
Si	TNAF.7	International Bit.
1	TNAF.6	Frame Non-Alignment Signal Bit.
A	TNAF.5	Remote Alarm.
Sa4	TNAF.4	Additional Bit 4.
Sa5	TNAF.3	Additional Bit 5.
Sa6	TNAF.2	Additional Bit 6.
Sa7	TNAF.1	Additional Bit 7.
Sa8	TNAF.0	Additional Bit 8.

12.0 LINE INTERFACE CONTROL FUNCTION

The DS2143 can control line interface units that contain serial ports. When Control Register Bytes 1 or 2 (CRB1, CRB2) are written to, the DS2143 will automatically write this data serially (LSB first) into the line interface by creating a chip select, serial clock and serial data via the LI_$\overline{CS}$, LI_SCLK and LI_SDI pins respectively. This control function is driven off of the RCLK and it must be present for proper operation. Registers CRB1 and CRB2 can only be written to, they cannot be read from. Writes to these registers must be at least 20 µs apart. See Section 13 for timing information.

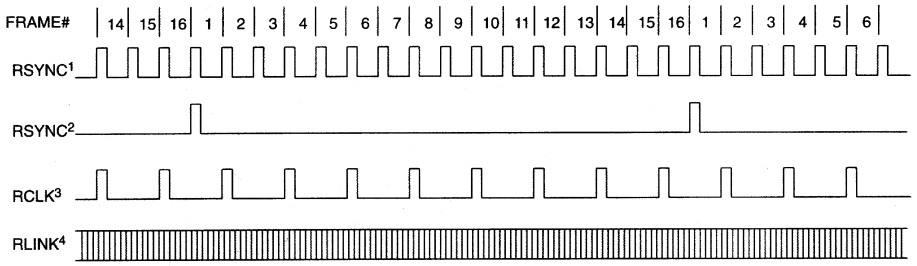
CRB1: CONTROL REGISTER BYTE 1 (Address=18 Hex)
CRB2: CONTROL REGISTER BYTE 2 (Address=19 Hex)

(MSB)							(LSB)	
CR7	CR6	CR5	CR4	CR3	CR2	CR1	CR0	CRB1
CR7	CR6	CR5	CR4	CR3	CR2	CR1	CR0	CRB2

SYMBOL	POSITION	NAME AND DESCRIPTION
CR1	CRB1.0	LSB of Control Register Byte 1.
CR7	CRB2.7	MSB of Control Register Byte 2.

13.0 TIMING DIAGRAMS

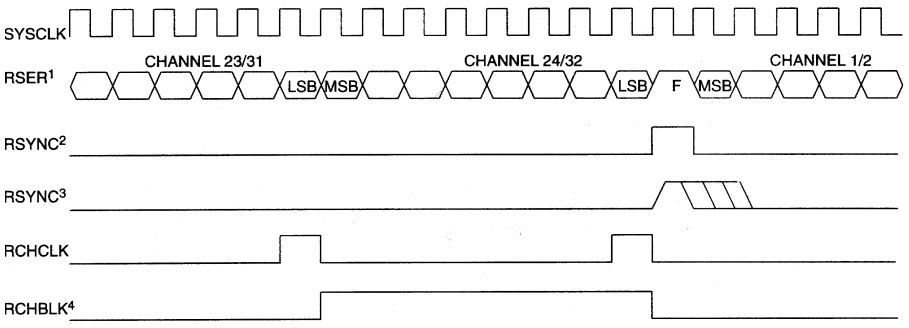
RECEIVE SIDE TIMING



NOTES:

1. RSYNC in the frame mode (RCR1.6=0).
2. RSYNC in the multiframe mode (RCR1.6=1).
3. RLCLK is programmed to output just the Sa4 bit.
4. RLINK will always output all 5 Sa bits as well as the rest of the receive data stream.
5. This diagram assumes the CAS MF begins with the FAS word.

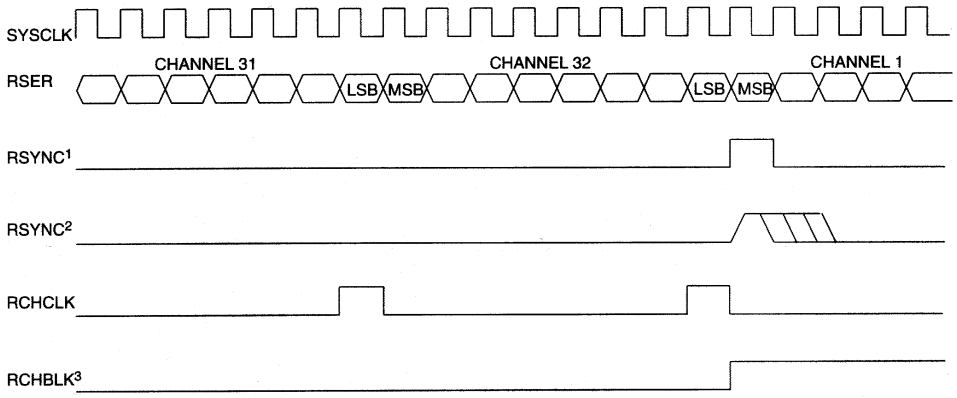
RECEIVE SIDE 1.544 MHZ BOUNDARY TIMING (WITH ELASTIC STORE ENABLED)



NOTES:

1. Data from the E1 channels 1, 5, 9, 13, 17, 21, 25, and 29 is dropped (channel 2 from the E1 link is mapped to channel 1 of the T1 link, etc.) and the F-bit position is added (forced to 1).
2. RSYNC is in the output mode (RCR1.5=0).
3. RSYNC is in the input mode (RCR1.5=1).
4. RCHBLK is programmed to block channel 24.

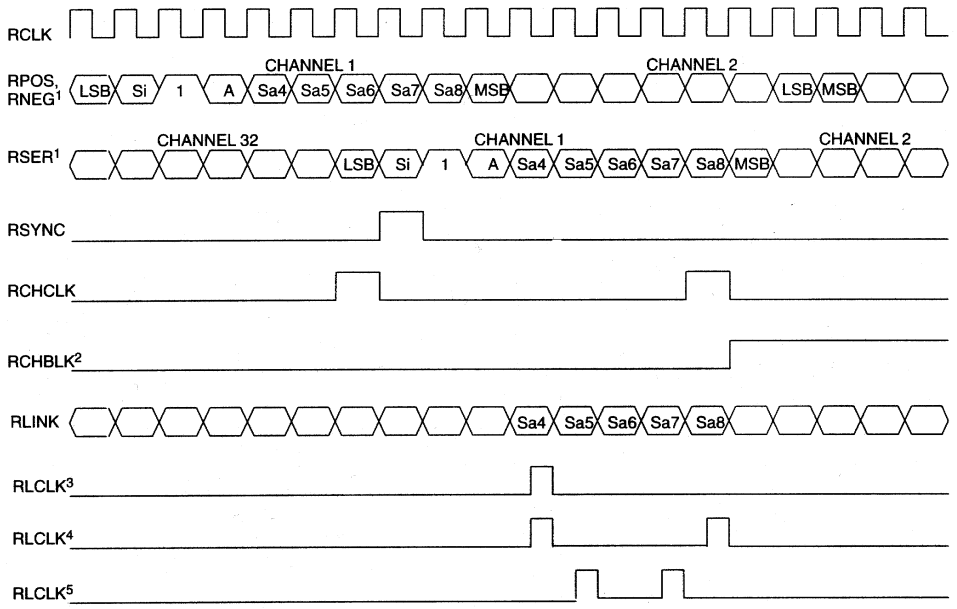
RECEIVE SIDE 2.048 MHZ BOUNDARY TIMING (WITH ELASTIC STORE ENABLED)



NOTES:

1. RSYNC is in the output mode (RCR1.5=0).
2. RSYNC is in the input mode (RCR1.5=1).
3. RCHBLK is programmed to block channel 1.

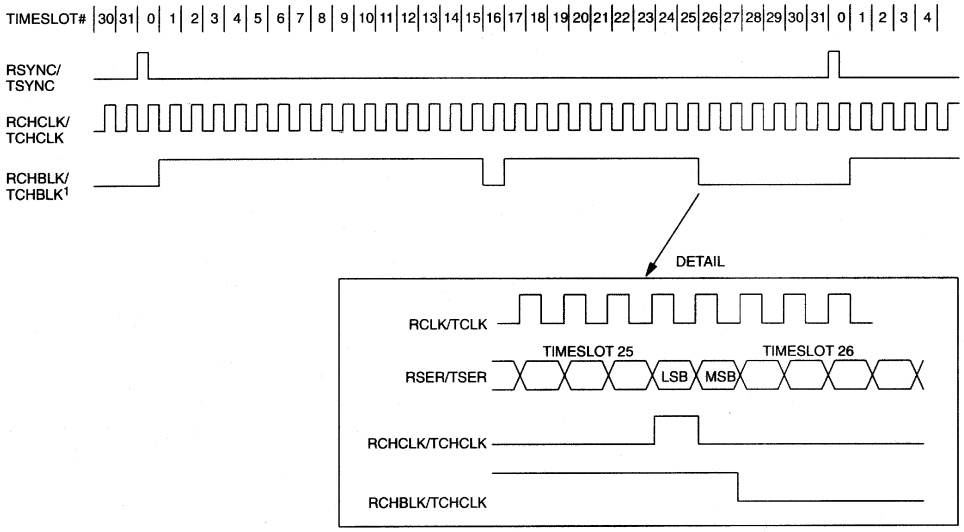
RECEIVE SIDE BOUNDARY TIMING (WITH ELASTIC STORE DISABLED)



NOTES:

1. There is a 6 RCLK delay from RPOS, RNEG to RSER.
2. RCHBLK is programmed to block channel 2.
3. RLINK is programmed to output the Sa4 bits.
4. RLINK is programmed to output the Sa4 and Sa8 bits.
5. RLINK is programmed to output the Sa5 and Sa7 bits.
6. Shown is a non-align frame boundary.

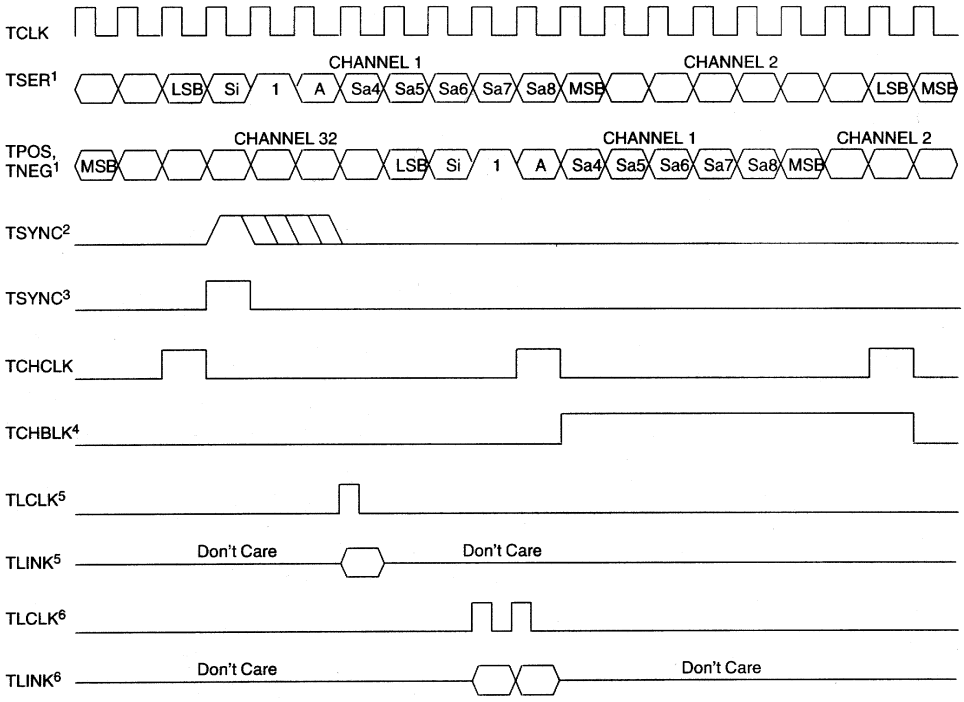
G.802 TIMING


TIMESLOT# 30 31 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 0 1 2 3 4
RSYNC/ TSYNC
RCHCLK/ TCHCLK
RCHBLK/ TCHBLK1
DETAIL
RCLK/TCLK
TIMESLOT 25
TIMESLOT 26
RSER/TSER
LSB
MSB
RCHCLK/TCHCLK
RCHBLK/TCHCLK

NOTE:

1. RCHBLK/TCHBLK is programmed to pulse high during timeslots 1 to 15, 17 to 25, during bit 1 of timeslot 26.

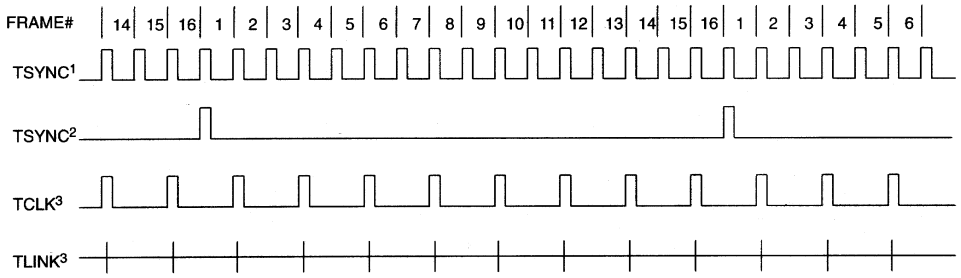
TRANSMIT SIDE BOUNDARY TIMING



NOTES:

1. There is a 5 TCLK delay from TSER to TPOS, and TNEG.
2. TSYNC is in the input mode (TCR1.0=0).
3. TSYNC is in the output mode (TCR1.0=1).
4. TCHBLK is programmed to block channel 2.
5. TLINK is programmed to source the Sa4 bits.
6. TLINK is programmed to source the Sa7 and Sa8 bits.
7. Shown is a non-align frame boundary.

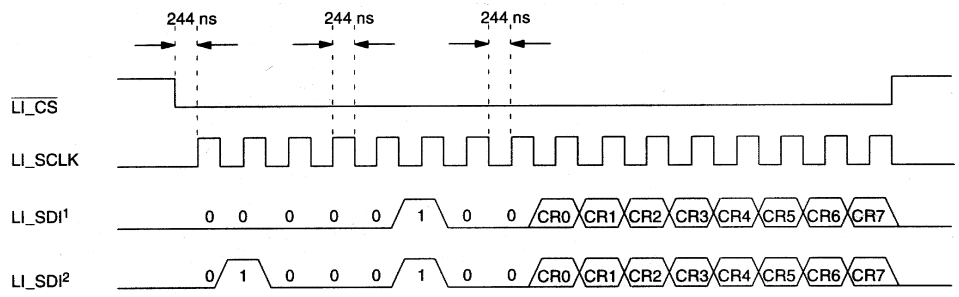
TRANSMIT SIDE TIMING



NOTES:

1. TSYNC in the frame mode (TCR1.1=0).
2. TSYNC in the multiframe mode (TCR1.1=1).
3. TLINK is programmed to source only the Sa4 bit.
4. This diagram assumes both the CAS MF and the CRC4 begin with the align frame.

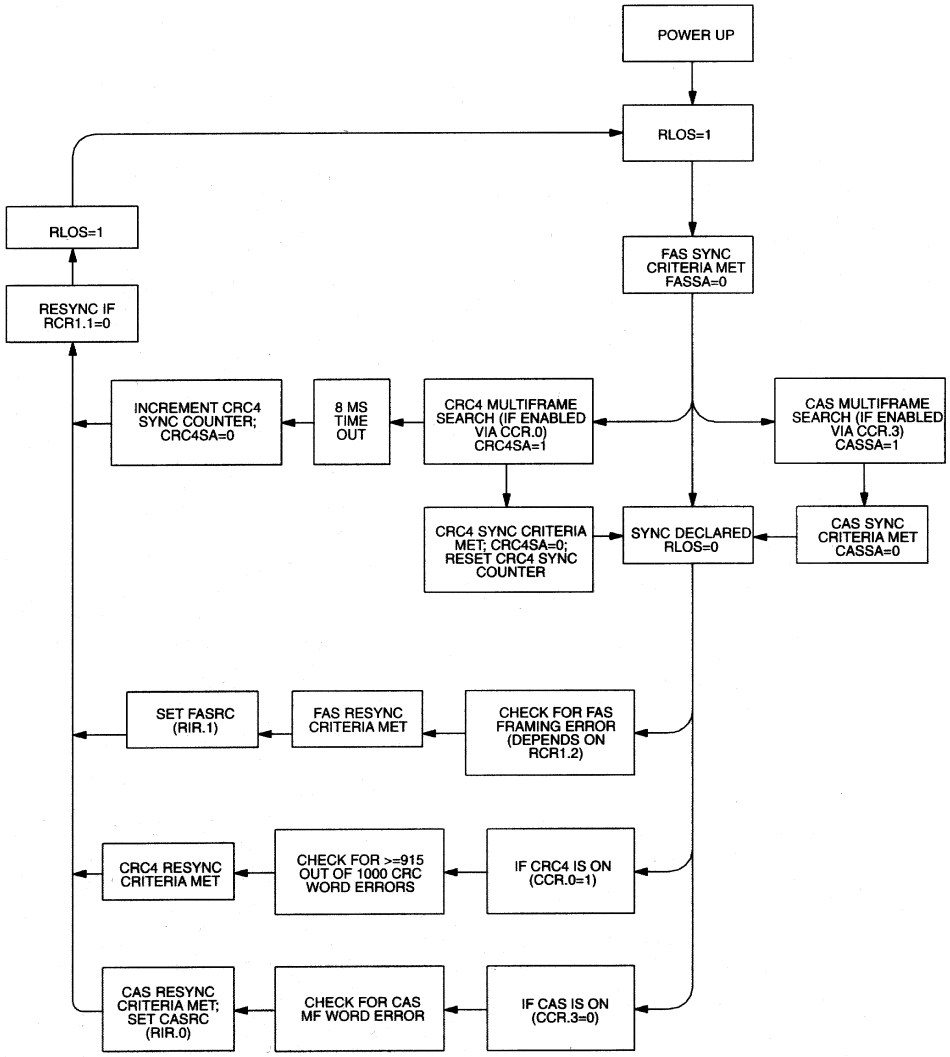
LINE INTERFACE CONTROL TIMING


244 ns
244 ns
244 ns
LI_CS
LI_SCLK
LI_SDI1
0 0 0 0 0 1 0 0 CR0 CR1 CR2 CR3 CR4 CR5 CR6 CR7
LI_SDI2
0 1 0 0 0 1 0 0 CR0 CR1 CR2 CR3 CR4 CR5 CR6 CR7

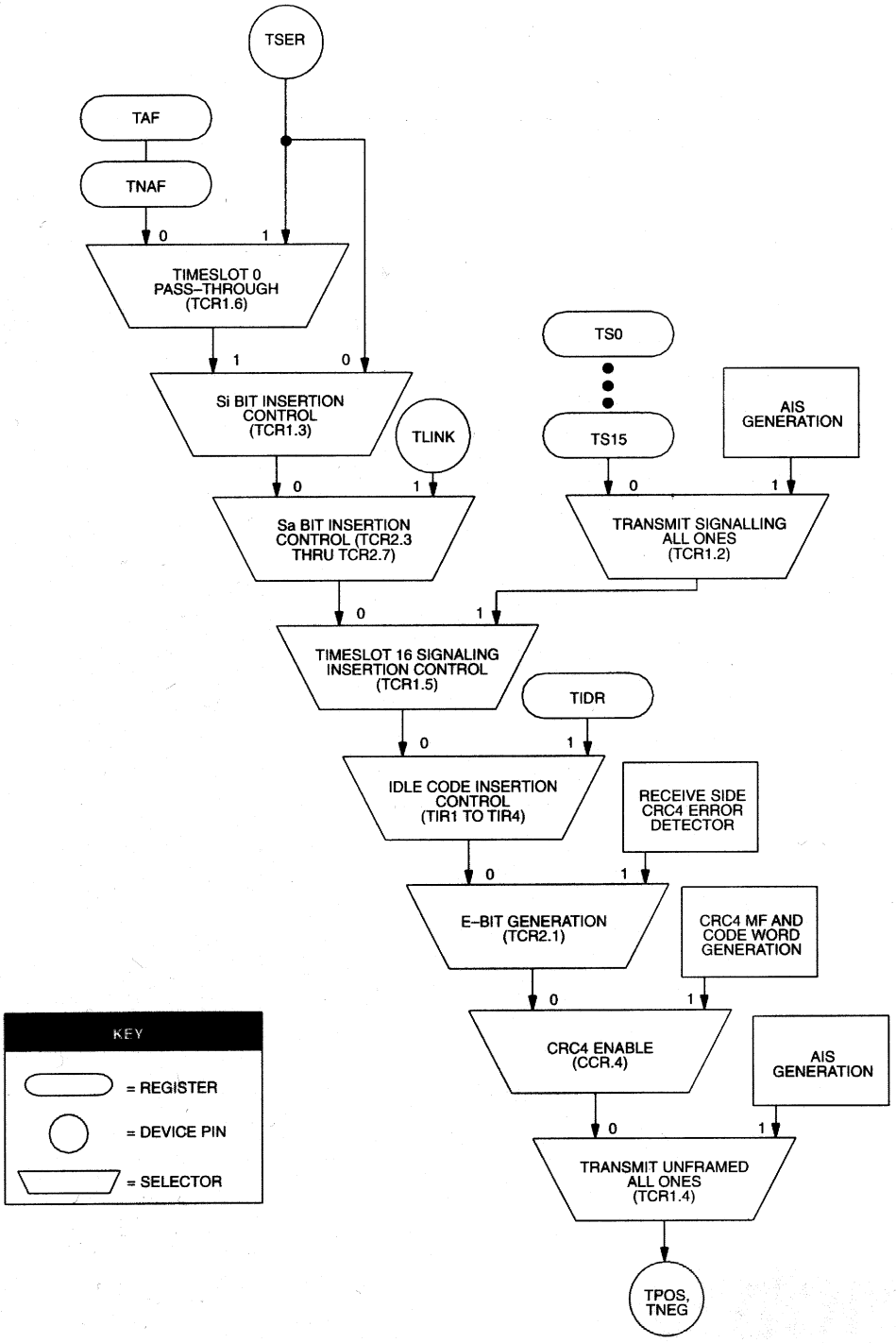
NOTES:

1. A write to CRB1 will cause the DS2143 to output this sequence.
2. A write to CRB2 will cause the DS2143 to output this sequence.
3. Timing numbers are based on RCLK=2.048 MHz with 50% duty cycle.

DS2143 SYNCHRONIZATION FLOWCHART


POWER UP
RLOS=1
FAS SYNC CRITERIA MET FASSA=0
CAS MULTIFRAME SEARCH (IF ENABLED VIA CCR.3) CASSA=1
CAS SYNC CRITERIA MET CASSA=0
SYNC DECLARED RLOS=0
CRC4 SYNC CRITERIA MET; CRC4SA=0; RESET CRC4 SYNC COUNTER
CRC4 MULTIFRAME SEARCH (IF ENABLED VIA CCR.0) CRC4SA=1
8 MS TIME OUT
INCREMENT CRC4 SYNC COUNTER; CRC4SA=0
RESYNC IF RCR1.1=0
RLOS=1
CHECK FOR FAS FRAMING ERROR (DEPENDS ON RCR1.2)
FAS RESYNC CRITERIA MET
SET FASRC (RIR.1)
IF CRC4 IS ON (CCR.0=1)
CHECK FOR >=915 OUT OF 1000 CRC WORD ERRORS
CRC4 RESYNC CRITERIA MET
IF CAS IS ON (CCR.3=0)
CHECK FOR CAS MF WORD ERROR
CAS RESYNC CRITERIA MET; SET CASRC (RIR.0)

DS2143 TRANSMIT DATA FLOW



ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	-1.0V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	-55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATION CONDITIONS (0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Logic 1	V_{IH}	2.0		V_{DD}+0.3	V	
Logic 0	V_{IL}	-0.3		+0.8	V	
Supply	V_{DD}	4.5		5.5	V	

CAPACITANCE

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}		5		pF	
Output Capacitance	C_{OUT}		7		pF	

DC CHARACTERISTICS (0°C to 70°C; V_{DD} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current	I_{DD}		10		mA	1
Input Leakage	I_{IL}	-1.0		+1.0	µA	2
Output Leakage	I_{LO}			1.0	µA	3
Output Current (2.4V)	I_{OH}	-1.0			mA	
Output Current (0.4V)	I_{OL}	+4.0			mA	

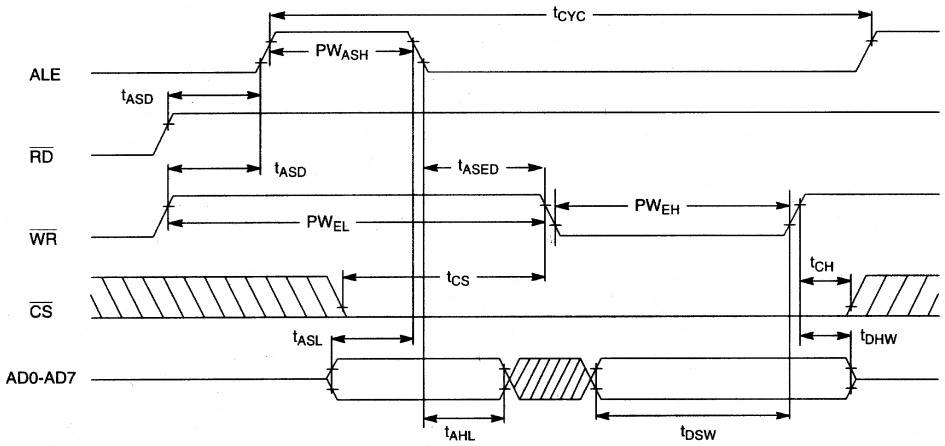
NOTES:

1. RCLK = TCLK = 2.048 MHz; V_{DD} = 5.5V.
2. 0.0V < V_{IN} < V_{DD}.
3. Applies to $\overline{INT1}$ and $\overline{INT2}$ when 3-stated.

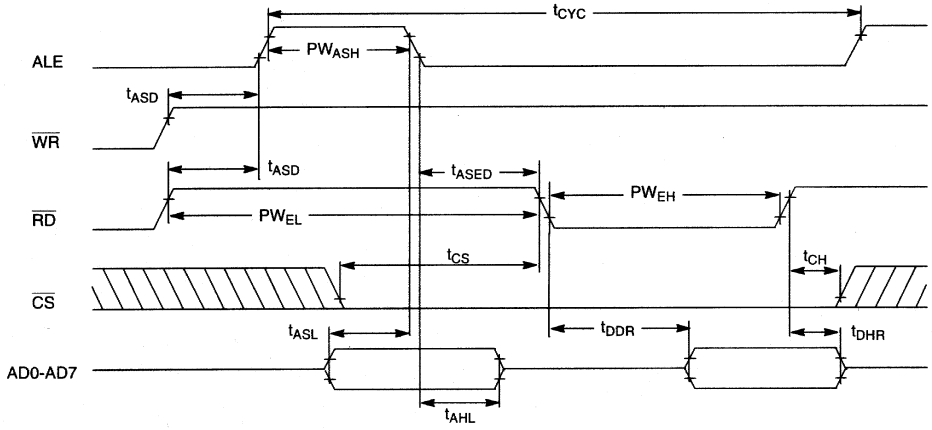
AC CHARACTERISTICS - PARALLEL PORT (0°C to 70°C; V_{DD} = 5V + 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Cycle Time	t_{CYC}	250			ns	
Pulse Width, DS Low or $\overline{RD}$ High	PW_{EL}	150			ns	
Pulse Width, DS High or $\overline{RD}$ Low	PW_{EH}	100			ns	
Input Rise/Fall Times	t_R, t_F			30	ns	
R/$\overline{W}$ Hold Time	t_{RWH}	10			ns	
R/$\overline{W}$ Setup Time Before DS High	t_{RWS}	50			ns	
$\overline{CS}$ Setup Time Before DS, $\overline{WR}$ or $\overline{RD}$ active	t_{CS}	20			ns	
$\overline{CS}$ Hold Time	t_{CH}	0			ns	
Read Data Hold Time	t_{DHR}	10		50	ns	
Write Data Hold Time	t_{DHW}	0			ns	
Muxed Address Valid to AS or ALE Fall	t_{ASL}	20			ns	
Muxed Address Hold Time	t_{AHL}	10			ns	
Delay Time, DS, $\overline{WR}$ or $\overline{RD}$ to AS or ALE Rise	t_{ASD}	25			ns	
Pulse Width AS or ALE High	PW_{ASH}	40			ns	
Delay Time, AS or ALE to DS, $\overline{WR}$ or $\overline{RD}$	t_{ASED}	20			ns	
Output Data Delay Time from DS or $\overline{RD}$	t_{DDR}	20		100	ns	
Data Setup Time	t_{DSW}	80			ns	

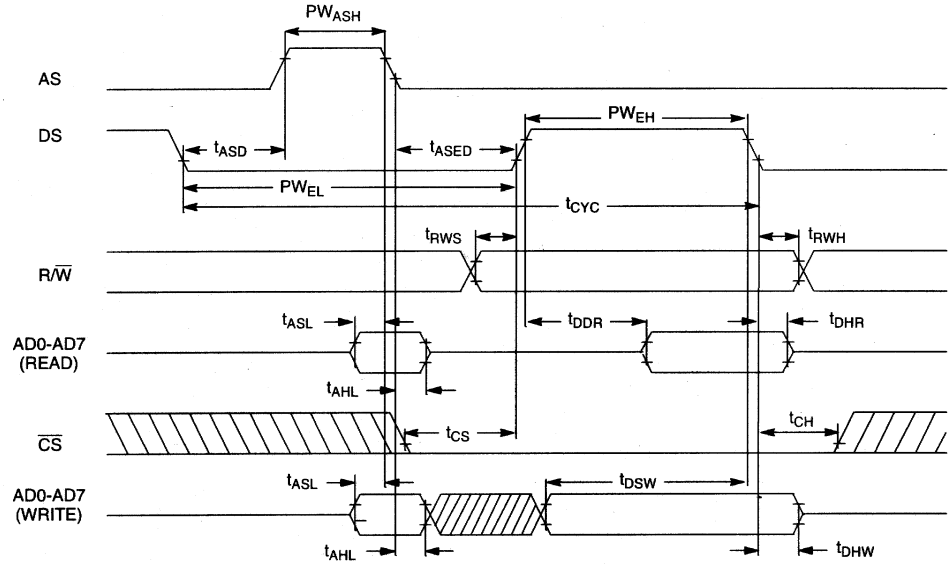
INTEL WRITE AC TIMING



INTEL READ AC TIMING



MOTOROLA AC TIMING



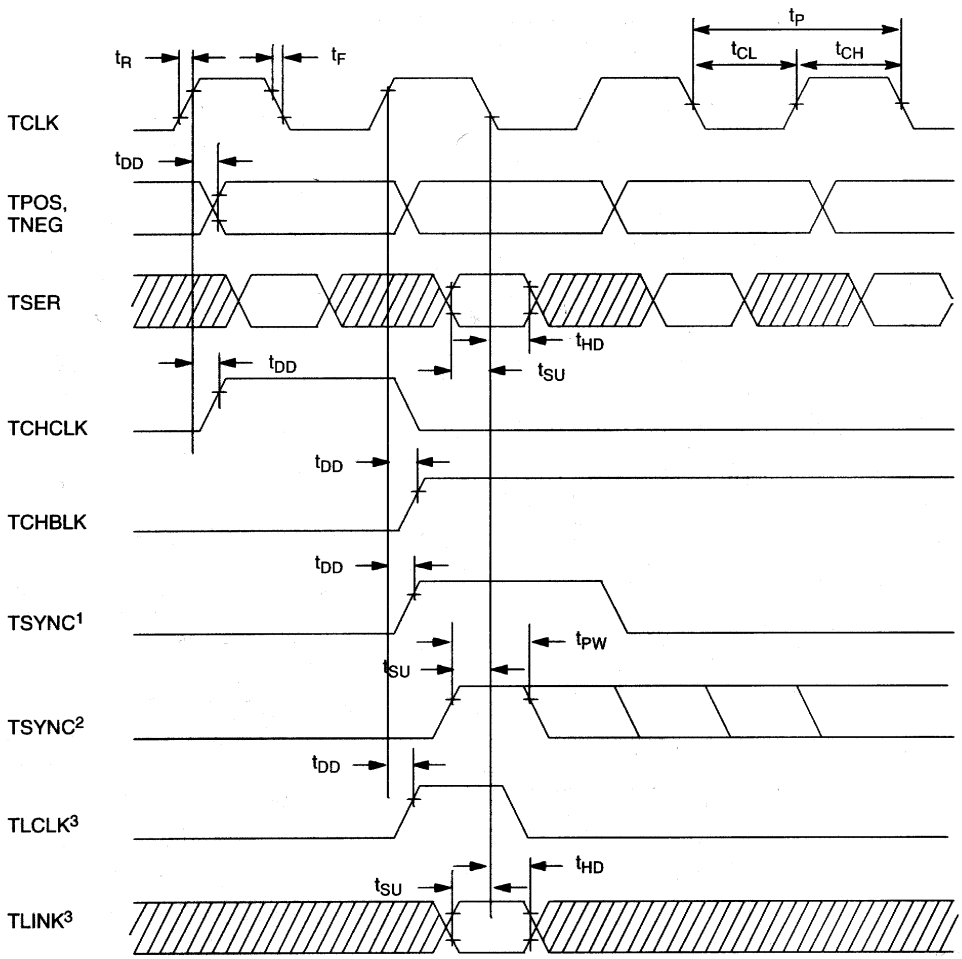
AC CHARACTERISTICS - TRANSMIT SIDE (0°C to 70°C; V_{DD} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
TCLK Period	t_P		488		ns	
TCLK Pulse Width	t_{CH} t_{CL}	50 50			ns ns	
TSER, TSYNC, TLINK Setup to TCLK Falling	t_{SU}	25			ns	
TSER, TLINK Hold from TCLK Falling	t_{HD}	25			ns	
TCLK Rise/Fall Times	t_R, t_F			25	ns	
Data Delay	t_{DD}			50	ns	
TSYNC Pulse Width	t_{PW}	50			ns	

AC CHARACTERISTICS - RECEIVE SIDE (0°C to 70°C; V_{DD} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
RCLK and SYSCLK Period	t_P		488		ns	
RCLK and SYSCLK Pulse Width	t_{CH} t_{CL}	50 50			ns ns	
RPOS, RNEG, RSYNC Setup to RCLK Falling	t_{SU}	25			ns	
RPOS, RNEG, Hold from RCLK Falling	t_{HD}	25			ns	
RCLK Rise/Fall Times	t_R, t_F			25	ns	
Data Delay	t_{DD}			60	ns	
RSYNC Pulse Width	t_{PW}	50			ns	

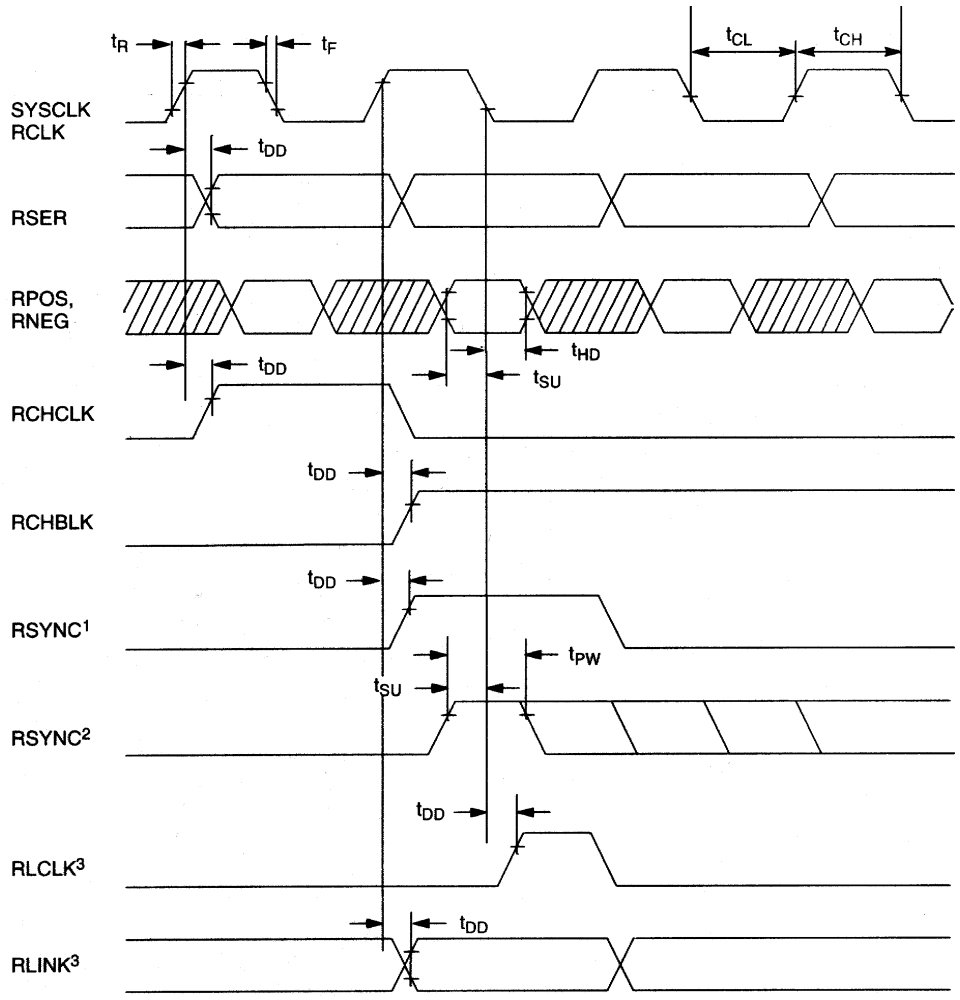
TRANSMIT SIDE AC TIMING



NOTES:

1. TSYNC is in the output mode (TCR1.0=1).
2. TSYNC is in the input mode (TCR1.0=0).
3. No timing relationship between TSYNC and TLCLK/TLINK is implied.

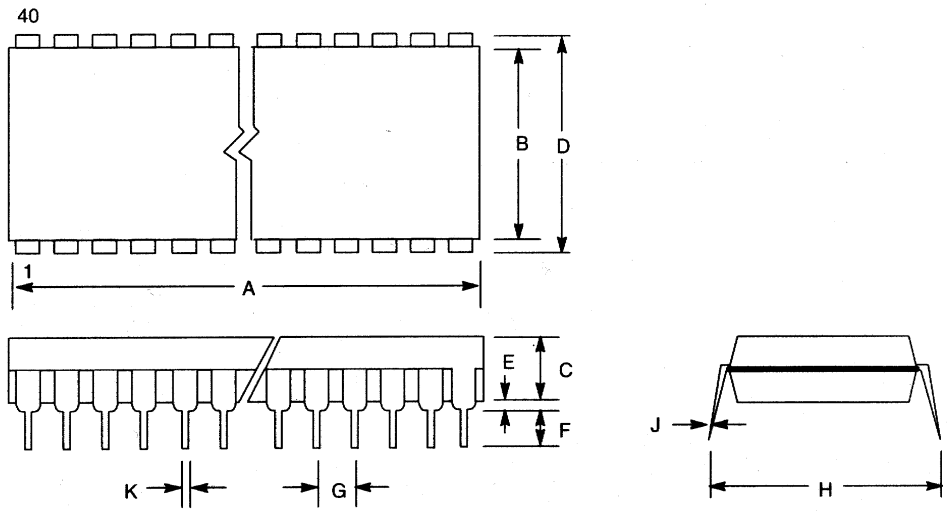
RECEIVE SIDE AC TIMING



NOTES:

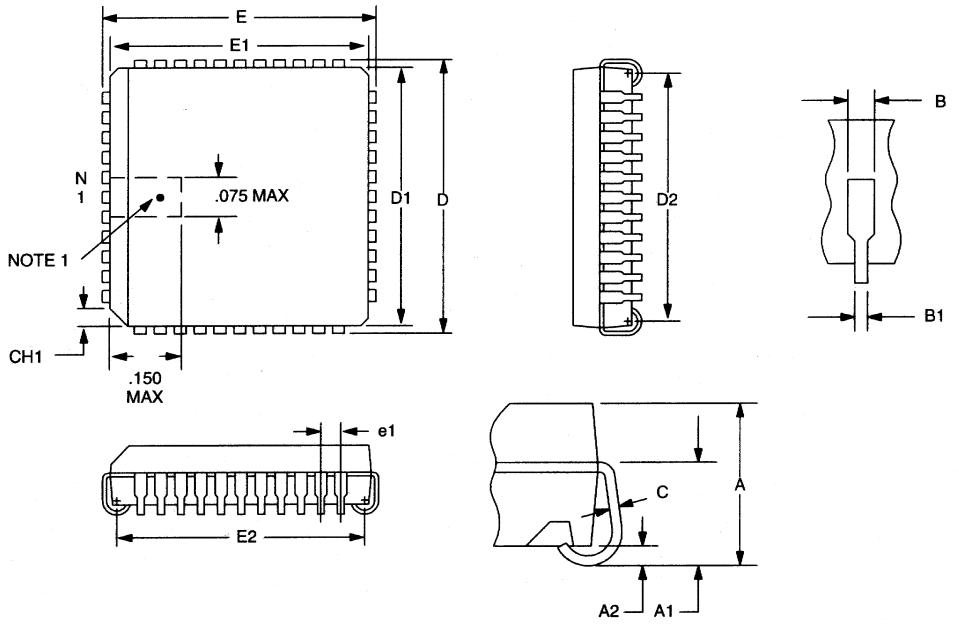
1. RSYNC is in the output mode (RCR1.5=0).
2. RSYNC is in the input mode (RCR1.5=1).
3. No timing relationship between RSYNC and RLCLK/RLINK is implied.

DS2143 E1 CONTROLLER (600 MIL) 40-PIN DIP



DIM	INCHES	
	MIN	MAX
A	2.040	2.070
B	0.530	0.560
C	0.145	0.155
D	0.600	0.625
E	0.015	0.040
F	0.120	0.140
G	0.090	0.110
H	0.625	0.675
J	0.008	0.012
K	0.015	0.022

DS2143 E1 CONTROLLER 44-PIN PLCC



NOTE1: PIN 1 IDENTIFIER TO BE LOCATED IN ZONE INDICATED.

DIM	INCHES	
	MIN	MAX
A	0.165	0.180
A1	0.090	0.120
A2	0.020	-
B	0.026	0.033
B1	0.013	0.021
C	0.009	0.012
CH1	0.042	0.048
D	0.685	0.695
D1	0.650	0.656
D2	0.590	0.630
E	0.685	0.695
E1	0.650	0.656
E2	0.590	0.630
e1	0.050 BSC	
N	44	-